# Silicon Vertex Trigger (SVT) Upgrade


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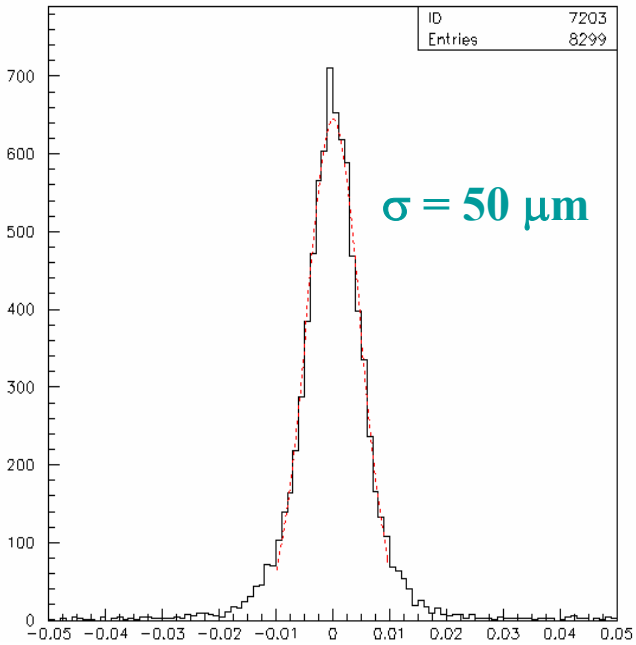
# Why SVT?

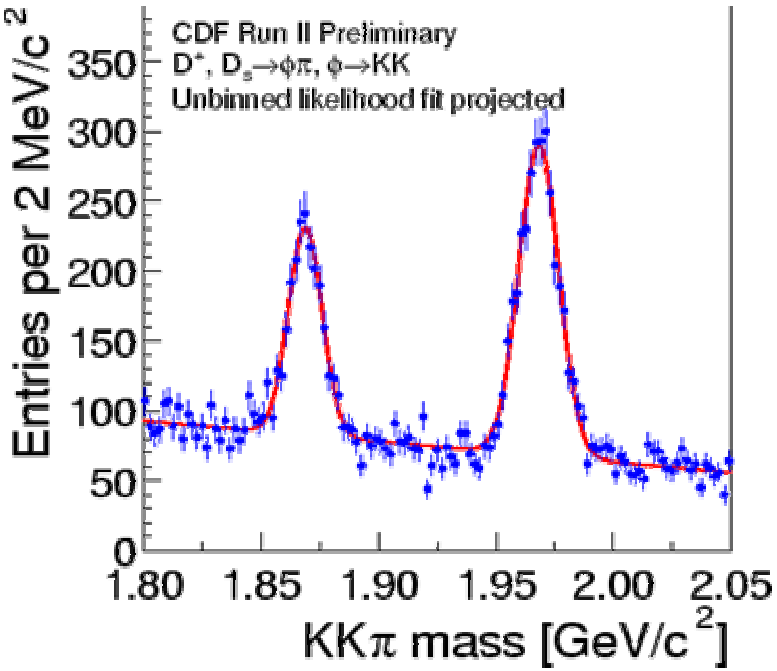
- **1st time at hadron collider:**

  **Trigger (~20 μsec) on *b* quarks based on lifetime.**

- **Important for both high-$P_T$ and *B* physics. (3rd generation)**
- **Attach to drift chamber tracks hits from silicon detector.**
- **Impact parameter resolution ≈ beam diameter.**

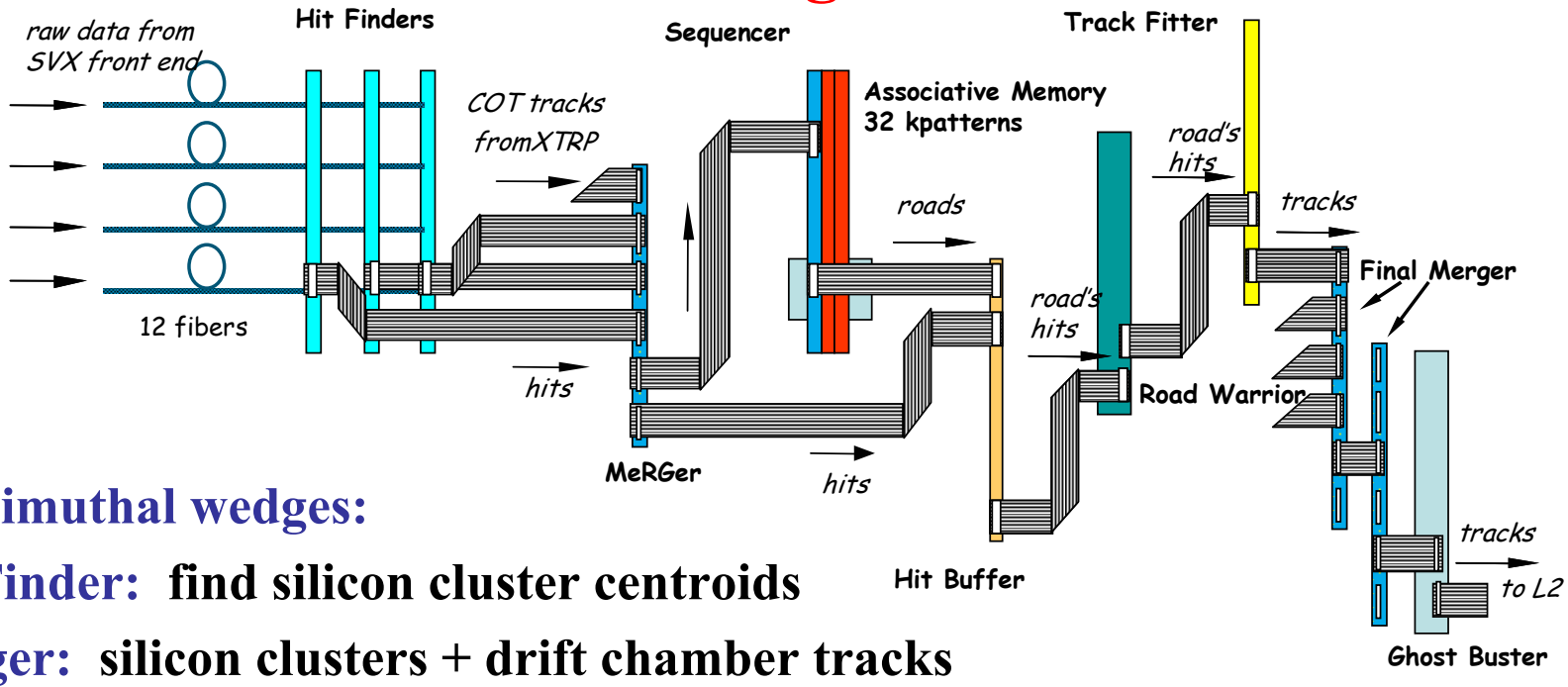



**impact parameter (cm)**




**1st CDF Run II paper: $D_s$-$D^+$ ΔM**

# The Existing SVT




**12 azimuthal wedges:**

**Hit Finder:** find silicon cluster centroids

**Merger:** silicon clusters + drift chamber tracks

**Associative Memory:** fast pattern recognition (32K patterns, "roads"/wedge)
uses coarser resolution ("superstrips" ~500μm)

**Hit Buffer:** stores hits at full resolution; retrieves those within a road

**Road Warrior:** remove roads with the same hits (important in 4/5 mode)

**Track Fitter:** fits track candidates with a linear approximation

**Ghost Buster:** keeps the best track associated with each drift chamber track

# Impact of SVT on the physics program

- **High $P_T$ physics:**
  - **Broad searches for new physics**
    - **High $P_T$ *b*-jet**
    - **Missing $E_T$ + *b*-jet**
    - **$\gamma$ + *b*-jet**
  - **Higgs search**
    - **Higgs multi-jet trigger**
  - **Top (and Higgs) mass**
    - $Z \rightarrow b\bar{b}$ **(with SVT trigger, 95% $b\bar{b}$ ; without SVT, <1%)**
- **B physics**
  - **All-hadronic final states ($B_s$ mixing, $\alpha$, …)**
    - **Multiple displaced tracks**
  - **Semi-leptonic tag**
    - **Lepton + displaced track**

# Why Upgrade SVT?

- **A critical issue for the trigger is deadtime.**

$$DT_{L2} \sim R_{L1} \times \overline{t}_{L2}$$

- **At current luminosities ( $< 10^{32}$), both high-$P_T$ and *B*- physics level-1 triggers have to be prescaled because of SVT execution time.**
- **At Run IIb luminosity, the level-1 rates become really big:**
  - **2-track *B* trigger: 49 KHz @ $1.5 \times 10^{32}$**
  - **$Z \rightarrow b\bar{b}$ trigger: 26 KHz @ $3 \times 10^{32}$**
- **There are many improvements under way for Run IIb.**
  - **L2 decision time**
  - **Detector → L3 transfer rate**
  - **L3 → Feynman Center transfer time**
- **Physics program limitation in Run IIb: SVT execution time**

# Preserving CDF Triggering Capability

- **Maintaining muon trigger acceptance in $1.0<|\eta|<1.5$.**
  - **XFT may require outer superlayer in Run IIb**
  - **$\Rightarrow$ trigger efficiency drops by ~ 50%**
  - **Using muon stubs as SVT seeds can restore the performance.**
- **Insurance against further COT degradation.**
  - **larger XFT fake rate $\Rightarrow$ more track candidates**
  - **worse pointing resolution $\Rightarrow$ need for more patterns**

# What to do about it

- **Reduce SVT execution time.**
  - **As luminosity ↑, SVX hit density ↑ (more with 396 nsec bunch spacing)**

    **⇒ more hits to process**

    **but more importantly**

    **⇒ more track candidates to fit because of the number of hits in a road**
  - **Reduce the road combinatorics by using narrower roads.**

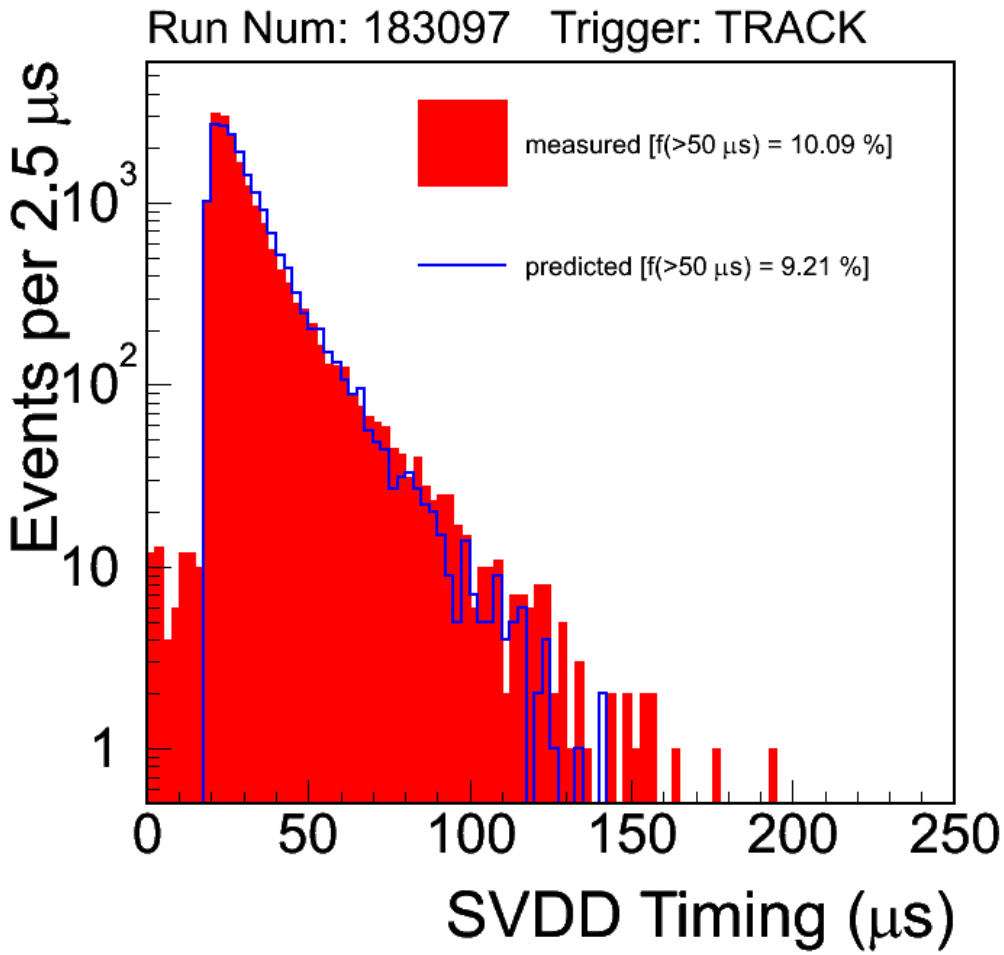
    **⇒ Increase the number of roads.**
  - **Reduce the fit execution time.**

    **⇒ Build a faster Track Fitter.**

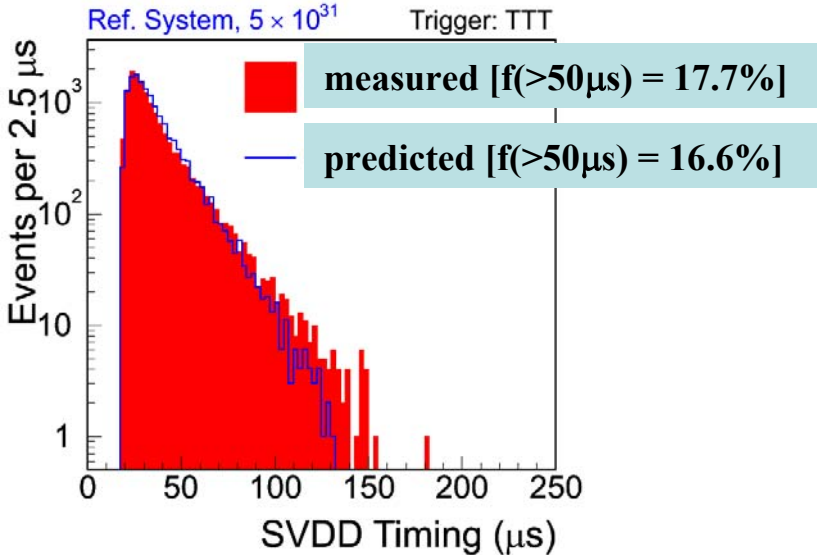
# How much improvement can we get?

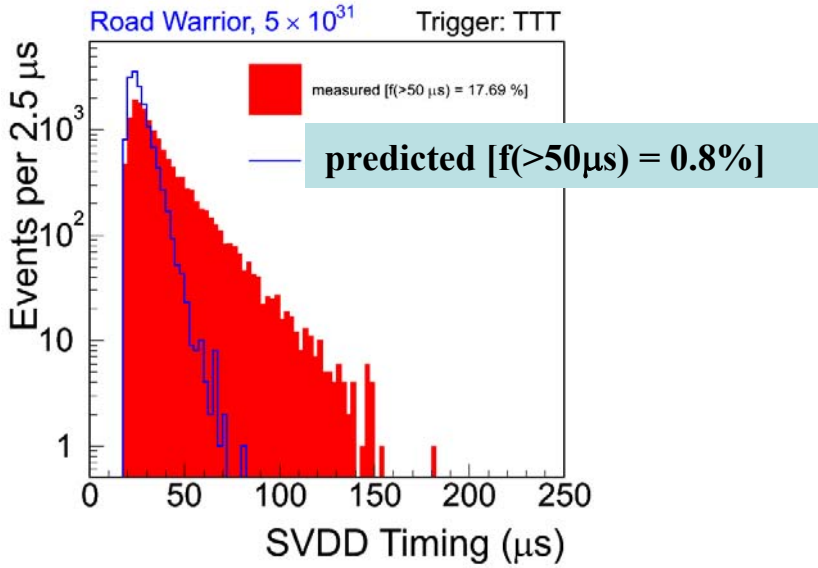
- **Model SVT timing:** $t_{SVT} = aN_{\text{hits}} + bN_{\text{comb}}$

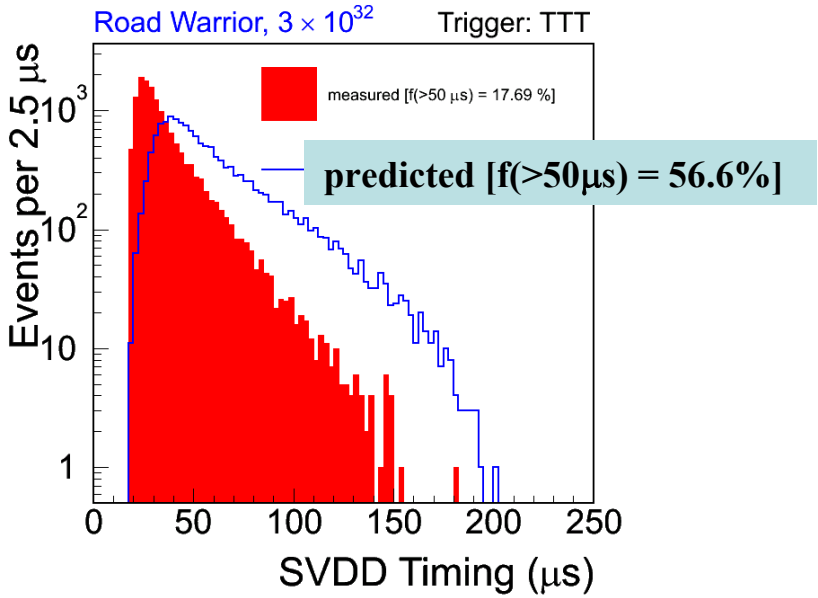
  **where $a$ and $b$ as well as $N_{\text{hits}}$ and $N_{\text{comb}}$ vs $\mathcal{L}$ are determined from data.**

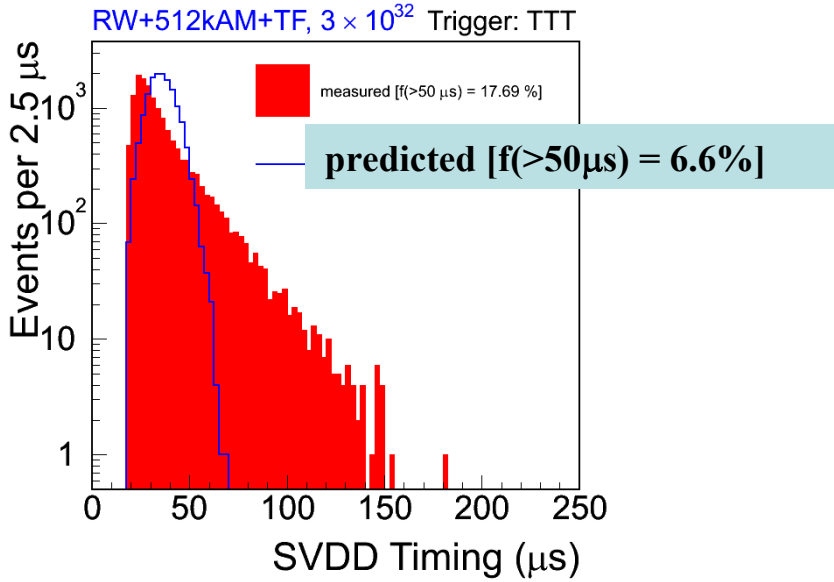


# Extrapolate to high $\mathcal{L}$ with & without upgrades

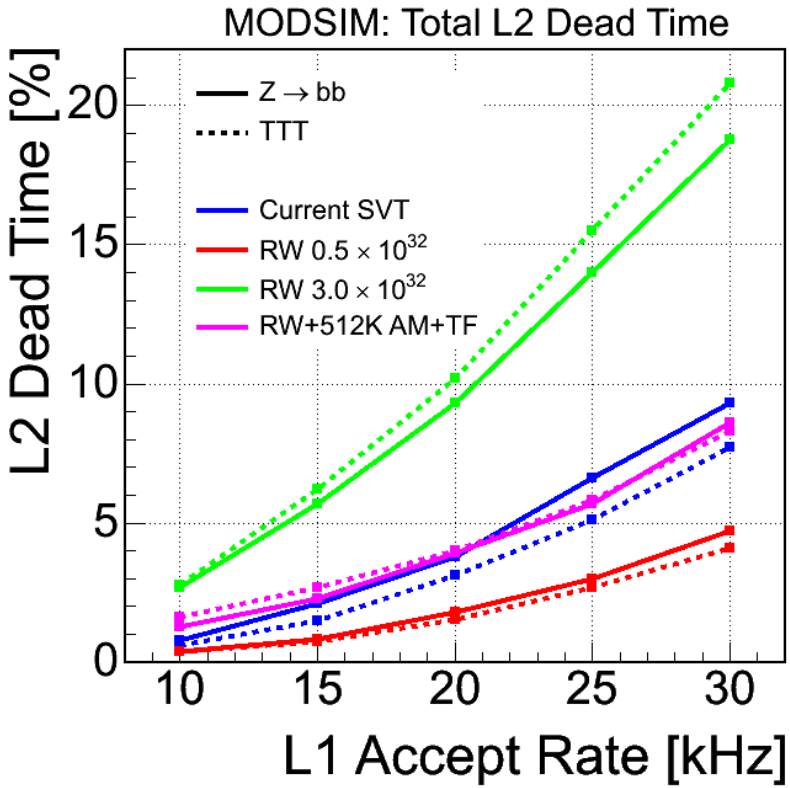


# What we could gain (after other trigger/DAQ upgrades)




← 5% deadtime

**Maximum L1 SVT-trigger rates for 5% L2 deadtime @ 3x10$^{32}$**

| Current SVT | Upgraded SVT |
|---|---|
| 13 KHz | 23 KHz |

# Specifically what will we do?

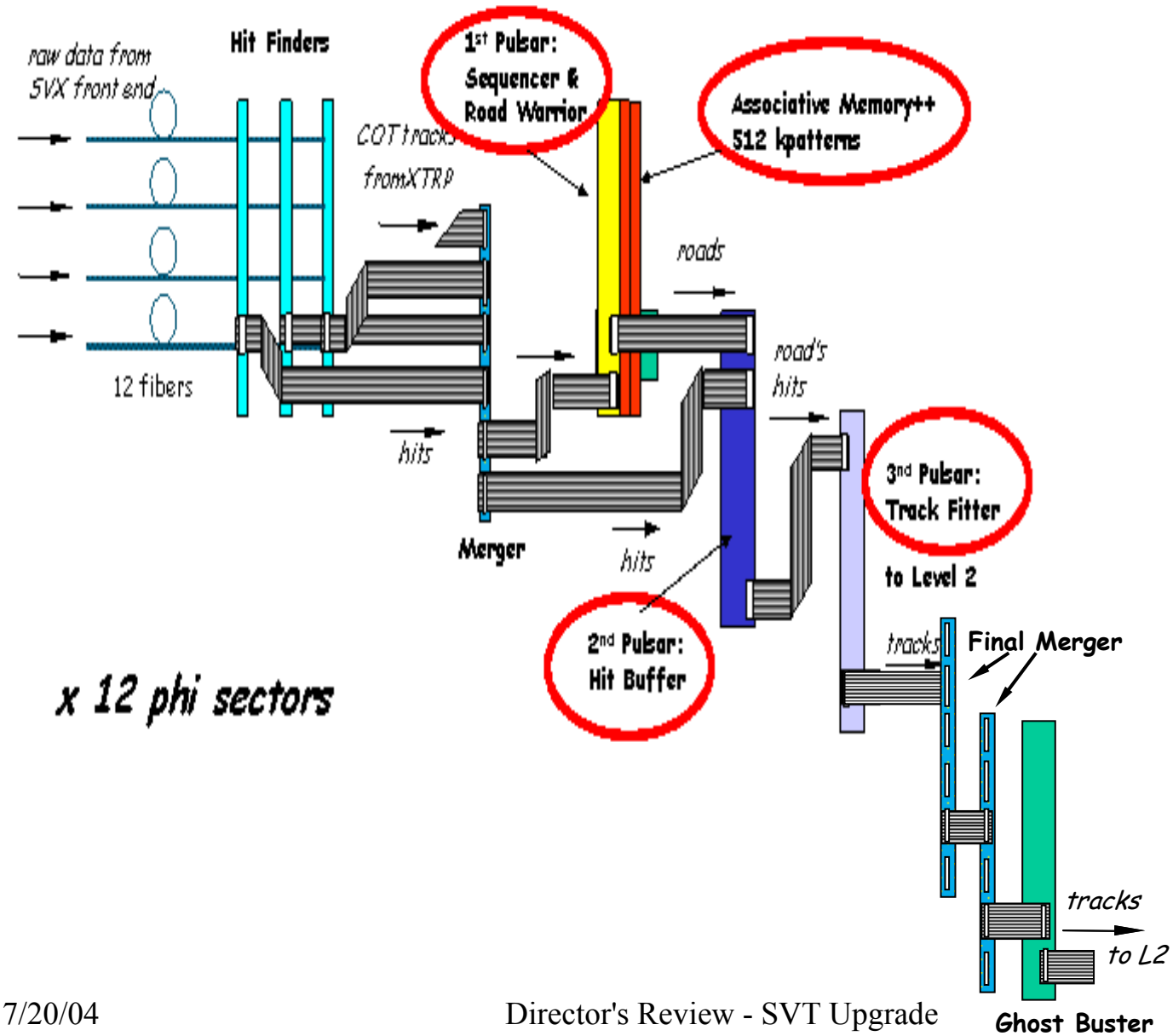
- **Build a minimum of new hardware.**

  **Use LHC design + new CDF Pulsar boards.**
  - **New Associative Memory (more roads)**
    - **Prototypes being constructed/tested (based on LHC design)**
    - **Sequencer firmware to be added to existing Road Warrior Pulsars.**
  - **New Hit Buffer (handle larger # of roads & faster)**
    - **Pulsar board with memory on mezzanine**
  - **New Track Fitter (handle larger # of roads & faster)**
    - **Pulsar board with memory on mezzanines**
- **$\Rightarrow$ Build Pulsar mezzanine cards.**

  **Write Pulsar firmware based on existing functionality.**

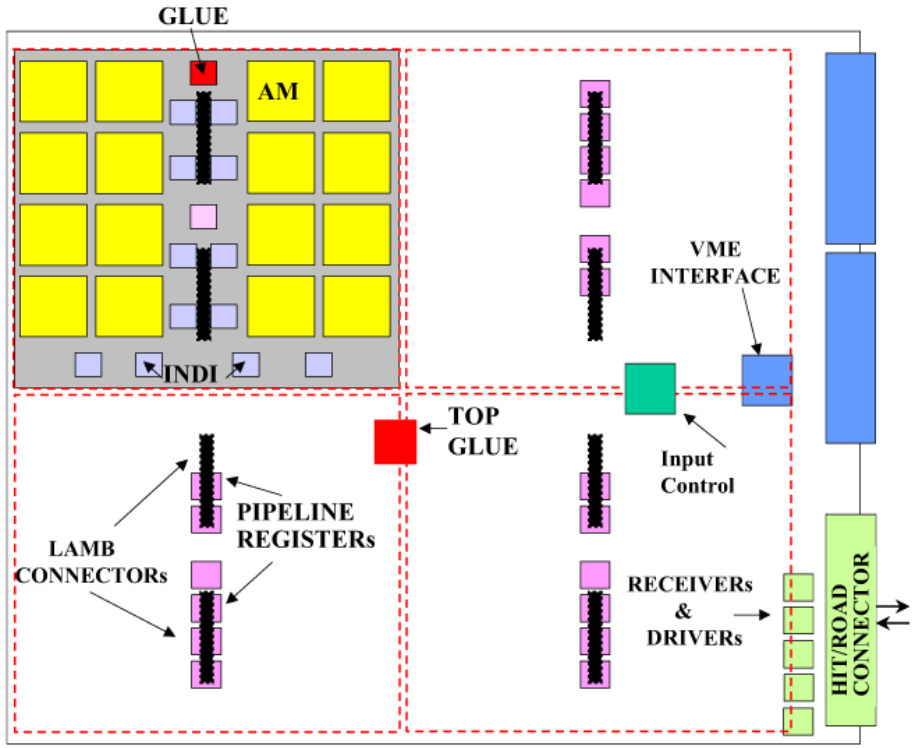
  **Upgrade online and offline software for new hardware.**

# The Upgraded SVT



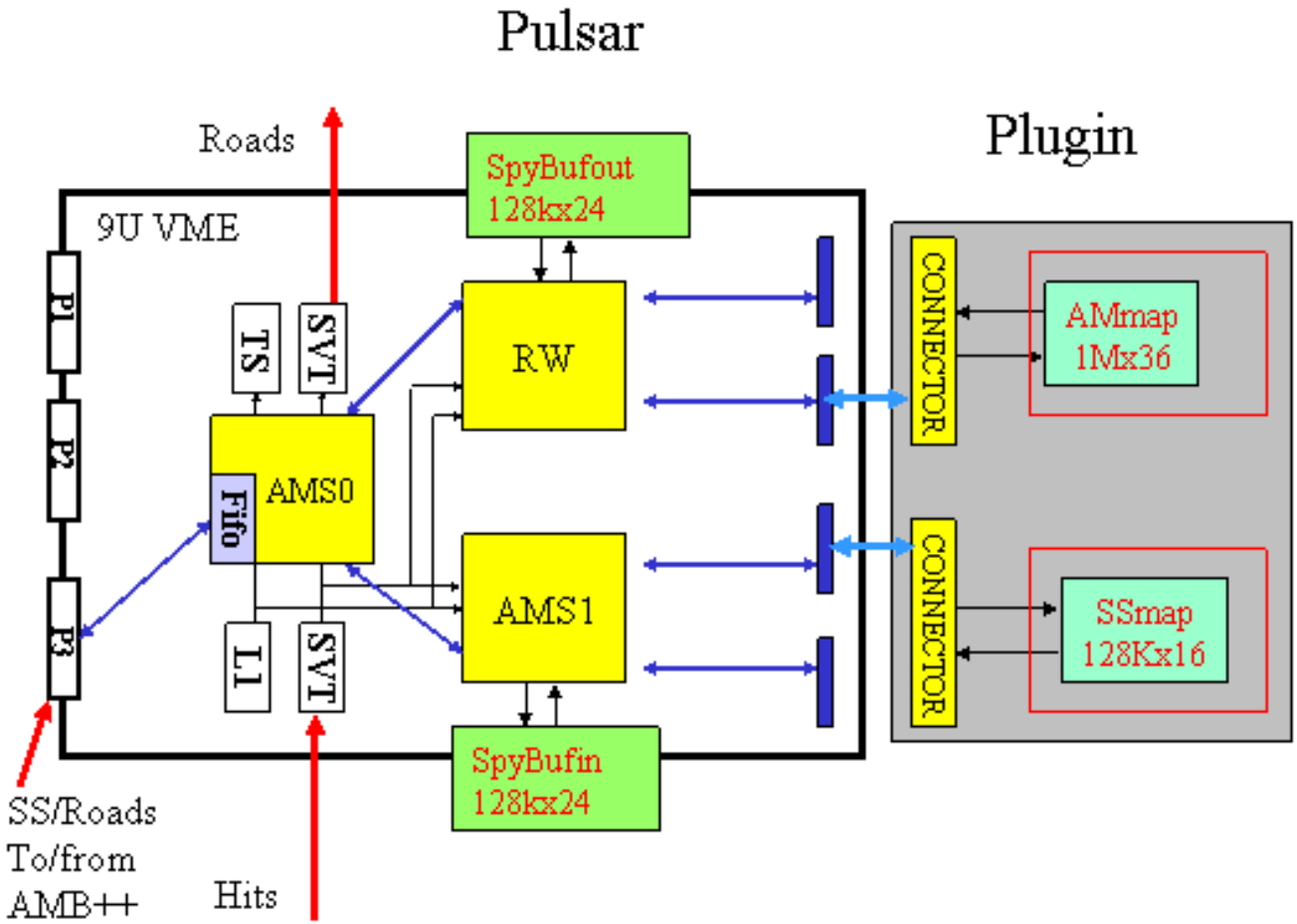
# New AM++ (fully funded by INFN)

- Track finding for all patterns simultaneously at high rate.
- AM chip: standard cell chip; prototype in production
- LAMB: prototype ready for testing with FPGA
- AM++: prototype testing begins next month



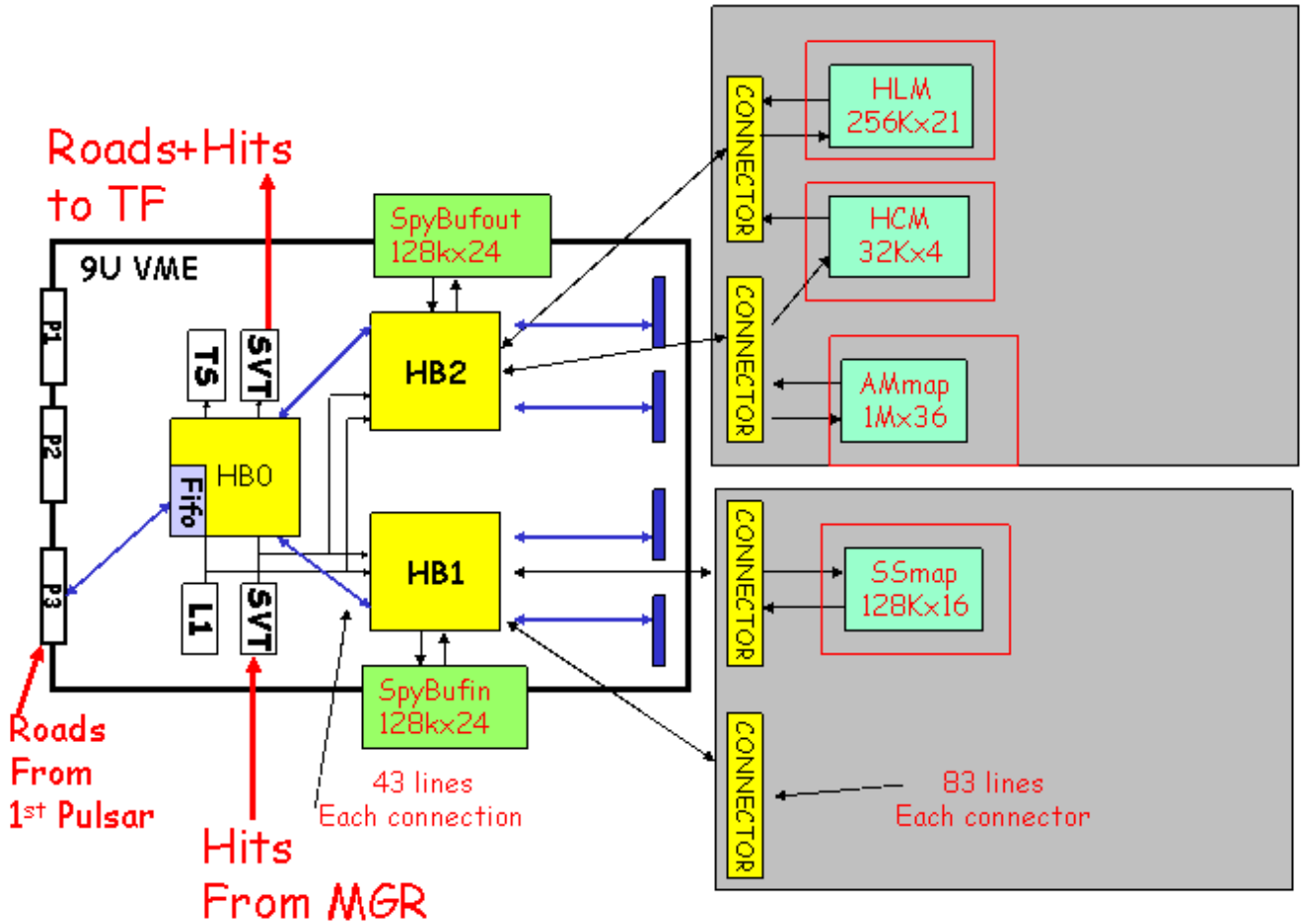
# AM Sequencer + Road Warrior

- **Pulsar board with firmware to be sequencer for AM system.**
- **Road Warrior function done before Hit Buffer. (speed)**
- **Need simple mezzanine card with memory.**



# Hit Buffer

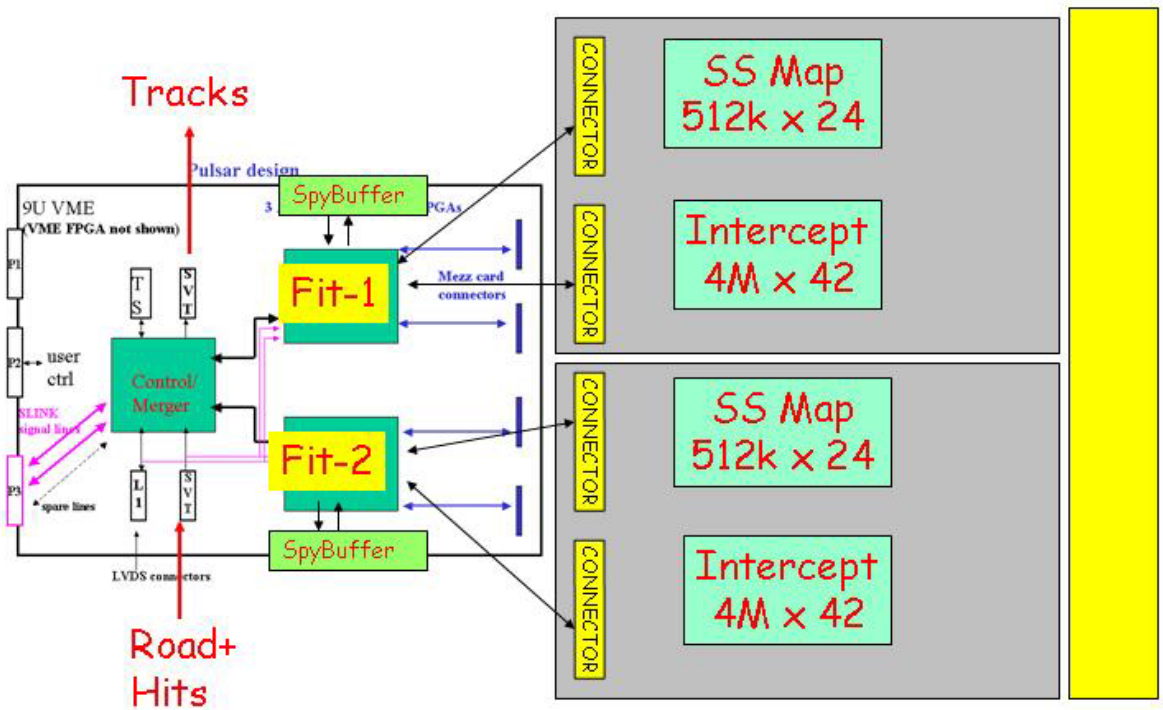
- **Hits stored with full resolution by superstrip.**
- **Roads sent by AMS/RW are sent out with raw hits attached.**
- **Pulsar board with HB firmware + mezzanines with memory.**



# Track Fitter

- **Receives a road and forms track candidates (combinations).**
- **Calculates *d*, *c*, φ, and fit $\chi^2$ using a linear approximation.**
- **Transmits tracks that pass a $\chi^2$ cut.**
- **Port existing Track Fitter firmware; build mezzanines.**

**Sketch of the Track Fitter**



# Software

- **Existing online and offline software has to be modified for the new hardware.**
  - **board simulation**
  - **creating roads and fitting constants**
  - **online diagnostics**
  - **online operating code (initialization)**
  - **readout code**
  - **offline tools**
  - **infrastructure, e.g. database code**

# Commissioning

- **Test stands exist at Fermilab, Pisa, and Chicago.**
- **First test boards at full speed in test stand with other Pulsars as transmitters and receivers.**
- **Test with CDF data without impacting normal data taking.**
  - **Existing SVT fanout boards can send data to new board with output compared to expectation.**
- **When Track Fitter is ready, it can be installed immediately to get speed advantage.**
- **When AM system, Hit Buffer, and Track Fitter are ready, they can all be installed.**

# US Cost
## (unburdened)

- Spares included
- Pulsar & transition cards identical to those built in the past few months
- Mezzanine cards based on recently built boards and price of chosen memory chip

| | | |
|---|---|---|
| • Pulsar boards | 28x$4.1K | $115K |
| • Mezzanine cards | total of 72 | 28K |
| • HB transition cards | 14 | 4K |
| • Cables & connectors | | 1K |
| • Mezzanine engineering | | 39K |
| • Firmware engineering | | 53K |
| | Total | $240K |

# Personnel

- **We have a large group of physicists working on SVT.**
- **No person is responsible for more than 1 item.**
- **Project management:** **M. Shochet, A. Annovi**
- **Coordination in Italy:** **P. Giannetti**

- **AM++:** **A. Bardi, L. Tripiccione, A. Annovi, P. Giovacchini, I. Ruffilli**
- **AMS/RW:** **F. Spinella, M. Piendibene**
- **Hit Buffer:** **I. Furic, T. Maruyama, T. Mansikkala (eng.)**
- **Track Fitter:** **J. Adelman, U. Yang**
- **Mezzanine:** **F. Tang (eng.), [M. Shochet]**
- **Software:** **Wisconsin group, M. Rescigno, A. Cerri, S. Donati, R. Carosi**

# Schedule Milestones

**( Pulsar boards will be ordered by October, 2004)**

| | | |
|---|---|---|
| • **AM++** | **begin production** | **01/05** |
| • **AMS/RW** | **firmware complete, full testing begins** | **05/05** |
| • **Hit Buffer** | **firmware complete, full testing begins** | **04/05** |
| • **Track Fitter** | **firmware complete, full testing begins** | **04/05** |
| • **Mezzanine cards** | **begin production** | **11/04** |
| • **SVT Upgrade ready for installation** | | **06/05** |

# Specifications Notes

| | |
|---|---|
| – AM++ chip | final version exists |
| – AM++ VME board | final version exists |
| – AM++ mezzanine card | final version exists |
| – AM mini-backplane board | final version exists |
| – common Pulsar mezzanine | draft exists; final by 8/15/04 |
| – AMS/RW I/O and firmware | final version exists |
| – Hit Buffer I/O and firmware | final version exists |
| – Track Fitter I/O and firmware | draft exists; final by 8/31/04 |
| – Software additions | task list exists |

# Conclusion

- **The SVT upgrade is important to the CDF Run II physics program.**
- **We have a design and a team that can complete the job on schedule.**
- **A significant fraction of the hardware is just copies of existing boards. Most of the rest is already in the prototype stage.**